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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,287	08/29/2000	Ted Chongpi Lee	Chi-1-1-5-1	9817

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EXAMINER	
PRIETO, BEATRIZ	

ART UNIT	PAPER NUMBER
2142	3

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,287 ✓	LEE ET AL.	
	Examiner	Art Unit	
	B. Prieto	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2000* . ✓

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final. ✓

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected. ✓

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This communication is in response to Application No. 09/650,287 filed 08/29/00, claims 1-20 are hereby set forth for examination.

2. Claim 2 recites the clause "said iteratively determined circuit path" on line 16, and further recites "said ideal path" and "said threshold level" on line 17 of page 14, show insufficient antecedent basis in the claim. Claims 3 and 5-6 recite the clauses "said ideal circuit path", claim 7 recites the clause "said circuit path" on line 9 and claim 8 recites the clause "said ideal path" on line 20, all show insufficient antecedent basis. Subsequent claims are replete with similar or other clauses having insufficient antecedent basis in their respective claims. Applicant is urged to review claims 1-20 for the these or similar lack of antecedent basis. Correction is required (see MPEP §2173.05(e)).

Claim Rejection 35 U.S.C. 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being by anticipated by DALEY et. al. (Daley) U.S. Patent No. 6,256,309.

Regarding claim 1, Daley teaches a system/method related to field of communication system,

teaching a system/method comprising the steps of:

iteratively defining a circuit path between a source node and a destination node in a network (Daley: repeatedly defining routes from a source node to a destination node, each defining a route i.e. physical link or virtual path connection between a source and each destination node, see col 1/lines 49-col 2/line 7, defining path from streams of destination nodes, col 5/lines 9-23, defining a circuit path (e.g. SVC) see col 2/lines 44-56), the network comprising

a plurality of nodes (12-16 of Fig. 1) interconnected by links, where each link has associated with it a respective bandwidth utilization level (Daley, bandwidth available see col 2/lines 63-67, path routes having range of available bandwidth see col 3/line 45-55) and

where links having bandwidth utilization levels exceeding a threshold level are not used to define said circuit path (Daley: do not use route if exceeding see col 8/lines 45-56, pruning, i.e. excluding routes for use see col 4/lines 50-65).

Regarding claim 2, prior art teaches the steps of:

determining a particular ("ideal") shortest path between the source node and destination node (Daley: calculate the shortest path (SPT) between a source and destinations see col 2/lines 44-56, calculate SPT see col 6/lines 5-16, computing shortest path according to a network constrains see col 3/lines 63-66);

comparing the particular ("ideal") shortest path to the iteratively defined circuit path (Daley: comparing the particular or each shortest path to a next shortest path associated with an multiple defined route paths and selecting the optimum shortest path see col 8/lines 50-58); and

in the case of said iteratively determined circuit path exceeding said ideal shortest path by a threshold amount (Daley: when determined shortest path for a defined circuit path exceeding said ideal shortest path by a value see col 8/lines 59-66);

adjusting said threshold level and repeating said step of iteratively defining said circuit path (Daley: shortest path optimization includes selecting among two paths, the optimum path e.g. the path having largest bandwidth see col 7/lines 65-col 8/line 9, each obtained shortest path route is compared with another shortest path until an accumulated optimized shorted path from all shortest path (i.e. adjusted or incremented threshold level) constrain value is generated see col 3/lines 45-58).

Regarding claim 3, said repeated shortest path defined circuit path is compared to said ideal shortest path defined circuit path by comparing the number of intervening nodes within each respective shortest path defined circuit path (Daley: shortest path optimized constraint sensitive

based constraint including number of hops see col 7/lines 65-col 8/line 8).

Regarding claim 4, wherein said threshold amount comprises a predetermined increase in the number of intervening nodes (Daley: shortest path optimization includes selecting among two paths, the optimum path e.g. largest bandwidth see col 7/lines 65-col 8/line 9, each obtained shortest path route is compared with another shortest path route until an accumulated optimized shorted path from all shortest path (i.e. adjusted or incremented constraint) is generated see col 8/lines 45-58).

Regarding claim 5, wherein said iteratively defined circuit path is compared to said ideal circuit path by comparing the latency within each respective circuit path (Daley: selection based on the shortest path route and the cell transfer delay see col 3/lines 63-col 4/line 11, selection based on a minimum delay see col 3/lines 46-55)

Regarding claim 6, wherein said iteratively defined circuit path is compared to said ideal circuit path by comparing the number of links within each respective circuit path (Daley: selection based on the shortest path route and minimum number of hops see col 7/lines 65-col 8/line 11).

Regarding claim 7, prior art further teaches

determining a shortest path between a source node and a destination node (Daley: shortest path determination computation see col 5/lines 16-34), said shortest path comprising a plurality of intervening nodes coupled by respective links (Daley, generate listing of available paths, see col 5/lines 16-34, calculated shortest path for a specified constraint see col 6/lines 6-16, constrains include number of hops to destination see column 6/lines 59-66);

determining whether a respective bandwidth utilization level for each link within said circuit path is below a threshold level (Daley: bandwidth thresholds see col 8/lines 27-50); and

adapting said circuit path to avoid using links having respective bandwidth utilization levels above said threshold level (Daley: pruning routes ("adapting"), i.e. pruning or excluding routes for use see col 4/lines 50-65, dropping links see col 2/lines 60-67)

Regarding claim 8, prior art further teaches

determining whether a circuit path formed using links having respective bandwidth utilization levels below said threshold level exceeds an ideal shortest circuit path by a threshold amount (Daley: col 8/lines 27-50, col 9/lines 27-44);

in the case of said circuit path exceeding said ideal path, adjusting said threshold levels and recalculating said circuit path (Daley: shortest path defining a circuit path, i.e. shortest path route compared with ideal shortest path route, adjusting threshold value, see col 8 lines 57-66).

Regarding claim 9, wherein said calculated circuit path is compared to said ideal circuit path in terms of at least one of a number of nodes within said circuit paths, a latency associated with communications within said circuit paths and a number of links within said circuit paths (Daley: shortest path selection including latency and number of hops .i.e. links see col 7/lines 65-col 8/line 9).

Regarding claim 10, prior art further teaches:

selecting, according to a shortest path algorithm, at least one link within a circuit path between a starting node and a destination node within a network comprising a plurality of nodes (Daley: path selection SPT based or choosing an SPT from among a plurality, each SPT associated with a route from one node to another node(s) see col 6/lines 1-29, selection of better path see col 8/lines 57-58);

determining whether each selected link has associated with it a bandwidth utilization level exceeding a threshold level (Daley: col 8/lines 26-50, see Fig. 4, step 62);

rejecting each selected link having associated with it a bandwidth utilization level exceeding said threshold level (Daley: col 8/lines 50-58); and

repeating said steps of selecting and determining until a circuit path between said starting node and said destination node has been determined (Daley: Fig. 4, step 60, a path selection for another see col 8/lines 57-58, repeating for each SPT select and determine steps see col 9/lines 3-14).

Regarding claim 11, increasing said threshold level in response to said determined circuit path exceeding an ideal circuit path by a predetermined amount (Daley: shortest path optimization includes selecting among two paths the path with the constraint e.g. largest bandwidth see col 7/lines 65-col 8/line 9, shortest paths computations are performed for a node and each destination nodes, each obtained shortest path route is compared with another until an accumulated optimized shorted path from all shortest path (i.e. adjusted or incremented constraint) is generated see col 8/lines 45-58).

Regarding claim 12, wherein said predetermined amount comprises a difference in one of the

number of nodes within said circuit paths, the latency associated with communications within said circuit paths and the number of links within said circuit paths (Daley: shortest path selection including number of hops and the cell transfer delay, i.e. latency see col 7/lines 65-col 8/line 8).

Regarding claim 13, selecting, according to said shortest path algorithm, each link within a circuit path between an intervening node (i.e. the last node of a partially formed circuit path) and said destination node (Daley: shortest path selection including number of hops see col 7/lines 65-col 8/line 8).

Regarding claim 14, this method claim contains limitation substantially the same as limitation discussed on the method claims 1, and 10, same rationale of rejection is applicable, further limitation include, selecting, according to a shortest path algorithm, an available link to a ("next") node within said circuit path (Daley: path selection SPT based or choosing an SPT from among a plurality, each SPT associated with a route from one node to another node(s) see col 6/lines 1-29, selection of better path see col 8/lines 57-58).

Regarding claim 15, determining if said circuit path exceeds an ideal circuit path by a predetermined amount; and in the case of said circuit path exceeding said ideal circuit by said predetermined amount, adjusting said threshold levels and repeating selecting, determining, rejecting and repeating steps discussed above (Daley: shortest path optimization includes selecting among two paths the path with the constraint e.g. largest bandwidth see col 7/lines 65-col 8/line 9, shortest paths computations are performed for a node and each destination nodes, each obtained shortest path route is compared with another until an accumulated optimized shorted path from all shortest path (i.e. adjusted or incremented constraint) is generated see col 8/lines 45-58).

Regarding claim 16, wherein said predetermined amount comprises a difference in one of the number of nodes within said circuit paths, the latency associated with communications within said circuit paths, and the number of links within said circuit paths (Daley: cell transfer delay and number of hops see col 7/lines 65-col 8/line 8).

Regarding claim 17, this claim comprises the computer readable medium storing a software program that, when executed by a computer, causes the computer to perform the method discussed on claim 1, therefore same rationale of rejection is applicable.

Regarding claim 18, this claim comprises the computer readable medium storing a software program that when executed by a computer causes the computer to perform the method discussed on claim 2, same rationale of rejection is applicable.

Regarding claim 19, prior art teaches:

a network manager for determining a circuit path between a source node and a destination node within a network comprising a plurality of nodes (Daley: routing agent 18 implements process of Fig. 2 for determining routes and associated available links between a source and destination nodes see col 5/lines 49-col 6/line 4, determining all circuit path e.g. virtual path or physical link between nodes see col 1/lines 49-col 2/lines 7); and

a data base for storing a respective bandwidth utilization level for each of a plurality of links interconnecting said nodes (Daley: database 22, stores obtained circuit path, i.e. typology information and associated traffic metrics see col 5/lines 38-62, routing table contain bandwidth utilization thresholds or brackets associated with available routes between nodes see col 5/lines 16-27;

said network manager determining said circuit path by iteratively selecting appropriate next nodes according to a shortest path algorithm (Daley: determining said circuit path by repeatedly selecting appropriate route to a destination node ("next nodes") according to a shortest path algorithm, generate listing of available paths according to the shortest path algorithm see col 5/lines 16-34, calculated shortest path for a specified constraint see col 6/lines 6-16, constrains include number of hops to destination see column 6/lines 59-66 next nodes or intervening nodes);

determining whether a link communicating with said selected next node has associated with it a bandwidth utilization level exceeding a threshold level (Daley, routing selection determine bandwidth available meeting requirements see col 2/lines 63-67, path routes selection having range of available bandwidth see col 3/line 45-55, links having bandwidth utilization levels exceeding a threshold level are not used to define said circuit path see col 8/lines 45-56, pruning, i.e. excluding routes for use see col 4/lines 50-65); and

selecting an alternative next node in the case of said link having associated with it a bandwidth utilization level exceeding said threshold level (Daley route selection must satisfy bandwidth requirements including selecting an alternative route that meet requirement col 5/lines 9-25, see route selection associated with bandwidth thresholds levels selection see col 8/lines 27-57 including select another route, alternative path selection see col 9/lines 3-16).

Regarding claim 20, in the case of a plurality of alternative next nodes having respective links

with bandwidth utilization levels above said threshold level, adjusting said threshold level (Daley: shortest path optimization includes selecting among two paths the path with the constrain e.g. largest bandwidth see col 7/lines 65-col 8/line 9, each obtained shortest path route is compared with another until an accumulated optimized shorted path from all shortest path (i.e. adjusted or incremented constraint) is generated see col 8/lines 45-58).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prieto, B. whose telephone number is (703) 305-0750. The Examiner can normally be reached on Monday-Friday from 6:00 to 3:30 p.m. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, Mark R. Powell can be reached on (703) 305-9703. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-6606. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800/4700.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
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or faxed to the Central Fax Office:

(703) 872-9306, for Official communications and entry;

Or Telephone:

(703) 306-5631 for TC 2100 Customer Service Office.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington VA, Fourth Floor (Receptionist), further ensuring that a receipt is provided stamped "TC 2100".

B. Prieto
TC 2100
Patent Examiner
September 28, 2003